AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

Please cancel claims 5, 7, 8 and 11 without prejudice. Please add new claims 21-24.

1. (CURRENTLY AMENDED) A method of verifying a repair of a design, comprising the steps of:

(A) generating an enumeration of a plurality of fuses in said design;

(B) compiling data for each of said fuses, wherein said data comprises simulation path data; ~~and~~

(C) automatically generating a repair file based on said simulation path data, said repair file predicting at least one of said fuses to implement said repair to a specific failure of said design;

(D) generating a repair program based on said repair file such that said at least one of said fuses simulates as programmed; and

~~(c)~~ (E) simulating said design with said at least one of said fuses programmed for said repair to verify said repair.

2. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein said simulation path data comprises verilog simulation path data.

3. (PREVIOUSLY PRESENTED) The method according to claim 14, wherein said schematic path data comprises at least one of a schematic path, a property, a hierarchy and a verilog path.

4. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein step (B) further comprises the sub-step of:

generating a list of layout coordinates and paths in said design as part of said compiling.

5. (CANCELLED)

6. (CURRENTLY AMENDED) The method according to claim ~~5~~ 1, further comprising the ~~step~~ steps of:

generating a fuse report; and

listing physical locations of a device in said design in response to said fuse report.

7. (CANCELED)

8. (CANCELED)

9. (CURRENTLY AMENDED) The method according to claim ~~8~~ 1, further comprising the step of:

verifying a function of said design in response to said repair program.

10. (CURRENTLY AMENDED) The method according to claim ~~8~~ 1, further comprising the step of:

listing an output of said repair program as a list of coordinates for said at least one of said fuses programmed for said repair in terms of a plurality of logical addresses.

11. (CANCELED)

12. (CURRENTLY AMENDED) An apparatus comprising:

a first circuit configured to enumerate a plurality of fuses in a design; and

a second circuit configured to (i) compile data for each of said fuses, wherein said data comprises simulation path data ~~and~~ (ii) generate a repair file based on said simulation path data, said repair file predicting at least one of said fuses to implement said repair to a specific failure of said design, (iii) generate a repair program based on said repair file such that said at least one of said fuses as programmed and (iv) perform a simulation said

design with said at least one of said fuses programmed for a repair of said design to verify said repair.

13. (CURRENTLY AMENDED) An apparatus comprising:

means for generating an enumeration of a plurality of fuses in a design;

means for (i) compiling data for each of said fuses, wherein said data comprises simulation path data~~; and~~ (ii) generating a repair file based on said simulation path data, said repair file predicting at least one of said fuses to implement said repair to a specific failure of said design, (iii) generating a repair program based on said repair file such that said at least one of said fuses as programmed and (iv) ~~means for~~ simulating said design with at least one of said fuses programmed for a repair of said design to verify said repair.

14. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein said data further comprises schematic path data.

15. (PREVIOUSLY PRESENTED) The method according to claim 1, wherein said data further comprises physical location data.

16. (PREVIOUSLY PRESENTED) The method according to claim 1, further comprising the step of:

mapping a plurality of co-ordinates of said fuses to a plurality of verilog program statements.

17. (CURRENTLY AMENDED) The method according to claim ~~8~~ 1, further comprising the step of:

checking ~~said repair file and~~ said repair program for an error in response to said repair failing in said simulation.

18. (PREVIOUSLY PRESENTED) The apparatus according to claim 12, wherein said first circuit is further configured to provide an elevation of said fuses at least one level of abstraction in said design.

19. (PREVIOUSLY PRESENTED) The apparatus according to claim 12, wherein said first circuit is further configured to collect data relevant to said fuses that are grouped.

20. (PREVIOUSLY PRESENTED) The apparatus according to claim 12, wherein said second circuit is further configured to write a report file.

21. (NEW) The method according to claim 1, further comprising the step of:

translating at least one coordinate in said repair file to at least one verilog programming statement of said design.

22. (NEW) The method according to claim 1, further comprising the step of:

verifying a plurality of fuse locations for said fuses against at least one identifiable shape drawn in a layout of said design.

23. (NEW) The method according to claim 1, further comprising the step of:

recording information identifying said fuses electrically connected in parallel to each other.

24. (NEW) The method according to claim 17, further comprising the step of:

checking said repair file for an error in response to both said repair failing in said simulation and said repair program having no errors.